74LVCV2G66

Overvoltage tolerant bilateral switch

Rev. 02 — 3 July 2008 **Product data sheet**

1. General description

The 74LVCV2G66 is a low-power, low-voltage, high-speed Si-gate CMOS device.

The 74LVCV2G66 provides two single pole single throw analog or digital switches. Each switch includes an overvoltage tolerant input/output terminal (pin nZ), an output/input terminal (pin nY) and low-power active HIGH enable input (pin nE).

The overvoltage tolerant switch terminals allow the switching of signals in excess of V_{CC}. The low-power enable input eliminates the necessity of using current limiting resistors in portable applications when using control logic signals much lower than V_{CC}. These inputs are also overvoltage tolerant.

2. Features

- Wide supply voltage range from 2.3 V to 5.5 V
- Ultra low-power operation
- Very low ON resistance:
  - 8.0 Ω (typical) at V_{CC} = 2.7 V
  - 7.5 Ω (typical) at V_{CC} = 3.3 V
  - 7.3 Ω (typical) at V_{CC} = 5.0 V.
- 5 V tolerant input for interfacing with 5 V logic
- High noise immunity
- Switch handling capability of 32 mA
- CMOS low-power consumption
- Latch-up performance exceeds 250 mA
- Incorporates overvoltage tolerant analog switch technology
- Switch accepts voltages up to 5.5 V independent of V_{CC}
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

founded by Philips

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVCV2G66DP	–40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVCV2G66DC	–40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVCV2G66GD	–40 °C to +125 °C	XSON8U	plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body 3 × 2 × 0.5 mm	SOT996-2

4. Marking

Table 2. Marking codes

Type number	Marking code
74LVCV2G66DP	Y66
74LVCV2G66DC	Y66
74LVCV2G66GD	Y66

5. Functional diagram

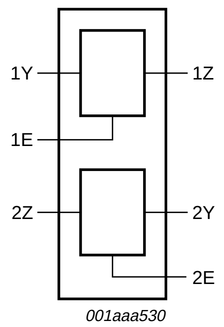


Fig 1. Logic symbol

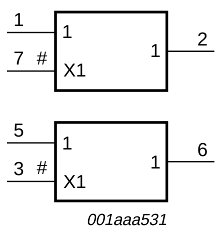


Fig 2. IEC logic symbol

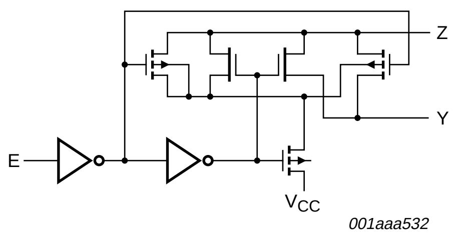


Fig 3. Logic diagram (one switch)

6. Pinning information

6.1 Pinning

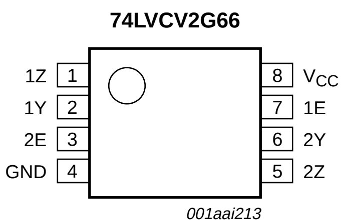


Fig 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

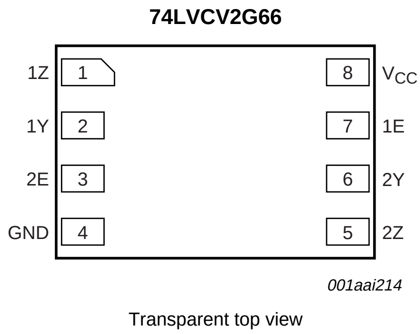


Fig 5. Pin configuration SOT996-2 (XSON8U)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
1Y, 2Y	2, 6	independent input or output
1Z, 2Z	1, 5	independent input or output (overvoltage tolerance)
GND	4	ground (0 V)
1E, 2E	7, 3	enable input (active HIGH)
V_{CC}	8	supply voltage

7. Functional description

Table 4: Function table[1]

Input nE	Switch
L	OFF-state
H	ON-state

[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+6.5	V
V_I	input voltage	[1]	–0.5	+6.5	V
I_{IK}	input clamping current	V_I < –0.5 V or V_I > 6.5 V	-	–50	mA
I_{SK}	switch clamping current	V_I < –0.5 V or V_I > 6.5 V	-	±50	mA

Table 5: Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{SW}	switch voltage	enable and disable mode		–0.5	+6.5	V
I_{SW}	switch current	V_{SW} > –0.5 V or V_{SW} < 6.5 V		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			–100	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.
For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.
For XSON8U package: above 45 °C the value of P_{tot} derates linearly with 2.4 mW/K.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage			2.3	-	5.5	V
V_I	input voltage			0	-	5.5	V
V_{SW}	switch voltage	enable and disable mode	[1]	0	-	5.5	V
T_{amb}	operating ambient temperature			–40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.3 V to 2.7 V	[2]	-	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	[2]	-	-	10	ns/V

[1] To avoid sinking GND current from terminal nZ when switch current flows in terminal nY, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no GND current will flow from terminal nY. In this case, there is no limit for the voltage drop across the switch.

[2] Applies to control signal levels.

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.3 V to 2.7 V		$0.6V_{CC}$	-	-	$0.6V_{CC}$	-	V
		V_{CC} = 3.0 V to 3.6 V		2.0	-	-	2.0	-	V
		V_{CC} = 4.5 V to 5.5 V		$0.55V_{CC}$	-	-	$0.55V_{CC}$	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.3 V to 2.7 V		-	-	$0.1V_{CC}$	-	$0.1V_{CC}$	V
		V_{CC} = 3.0 V to 3.6 V		-	-	0.5	-	0.5	V
		V_{CC} = 4.5 V to 5.5 V		-	-	$0.15V_{CC}$	-	$0.15V_{CC}$	V
I_I	input leakage current	pin nE; V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	[2]	-	±0.1	±5	-	±5	µA

Table 7. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

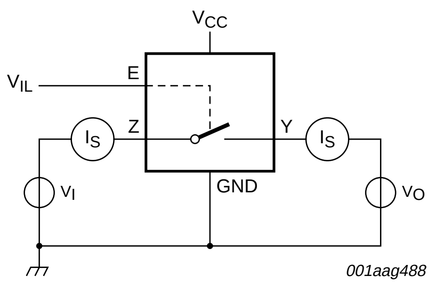
Symbol	Parameter	Conditions		−40 °C to +85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
$I_{S(OFF)}$	OFF-state leakage current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 2.3 V to 5.5 V; see Figure 6	[2][3]	-	±0.1	±10	-	±10	μA
$I_{S(ON)}$	ON-state leakage current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 2.3 V to 5.5 V; see Figure 7	[2][3]	-	±0.1	±10	-	±10	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; V_{SW} = GND or V_{CC}; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	[2]	-	0.1	10	-	40	μA
ΔI_{CC}	additional supply current	pin nE; $V_I = V_{CC} - 0.6$ V; V_{SW} = GND or V_{CC}; I_O = 0 A; V_{CC} = 3.0 V to 5.5 V	[2]	-	0.1	5	-	50	μA
C_I	input capacitance			-	2.5	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance			-	8.0	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance			-	16	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

[2] These typical values are measured at V_{CC} = 3.3 V.

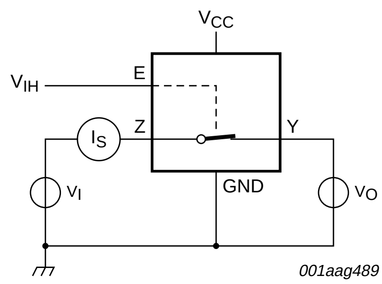
[3] For overvoltage signals ($V_{SW} > V_{CC}$) the condition $V_Y < V_Z$ must be observed.

10.1 Test circuits



V_I = GND and V_O = GND or 5.5 V.

Fig 6. Test circuit for measuring OFF-state leakage current



V_I = 5.5 V or GND and V_O = open circuit.

Fig 7. Test circuit for measuring ON-state leakage current

10.2 ON resistance

Table 8. Resistance R_{ON}

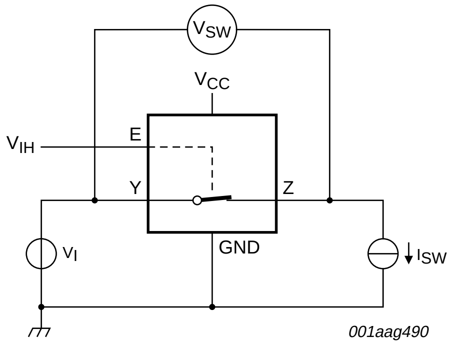
At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see Figure 9 and Figure 10.

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	V_{SW} = GND to V_{CC}; $V_I = V_{IH}$; see Figure 8						
		I_{SW} = 8 mA; V_{CC} = 2.3 V to 2.7 V	-	13	30	-	30	Ω
		I_{SW} = 12 mA; V_{CC} = 2.7 V	-	10	25	-	25	Ω
		I_{SW} = 24 mA; V_{CC} = 3.0 V to 3.6 V	-	8.3	20	-	20	Ω
		I_{SW} = 32 mA; V_{CC} = 4.5 V to 5.5 V	-	7.4	15	-	15	Ω
$R_{ON(rail)}$	ON resistance (rail)	V_{SW} = GND; $V_I = V_{IH}$; see Figure 8						
		I_{SW} = 8 mA; V_{CC} = 2.3 V to 2.7 V	-	8.5	20	-	20	Ω
		I_{SW} = 12 mA; V_{CC} = 2.7 V	-	8.0	18	-	18	Ω
		I_{SW} = 24 mA; V_{CC} = 3.0 V to 3.6 V	-	7.5	15	-	15	Ω
		I_{SW} = 32 mA; V_{CC} = 4.5 V to 5.5 V	-	7.3	10	-	10	Ω
		$V_{SW} = V_{CC}$; $V_I = V_{IH}$						
		I_{SW} = 8 mA; V_{CC} = 2.3 V to 2.7 V	-	8.5	20	-	20	Ω
		I_{SW} = 12 mA; V_{CC} = 2.7 V	-	7.2	18	-	18	Ω
		I_{SW} = 24 mA; V_{CC} = 3.0 V to 3.6 V	-	6.5	15	-	15	Ω
		I_{SW} = 32 mA; V_{CC} = 4.5 V to 5.5 V	-	5.7	10	-	10	Ω
$R_{ON(flat)}$	ON resistance (flatness)	V_{SW} = GND to V_{CC}; $V_I = V_{IH}$ [2]						
		I_{SW} = 8 mA; V_{CC} = 2.5 V	-	17	-	-	-	Ω
		I_{SW} = 12 mA; V_{CC} = 2.7 V	-	10	-	-	-	Ω
		I_{SW} = 24 mA; V_{CC} = 3.3 V	-	5	-	-	-	Ω
		I_{SW} = 32 mA; V_{CC} = 5.0 V	-	3	-	-	-	Ω

[1] All typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.

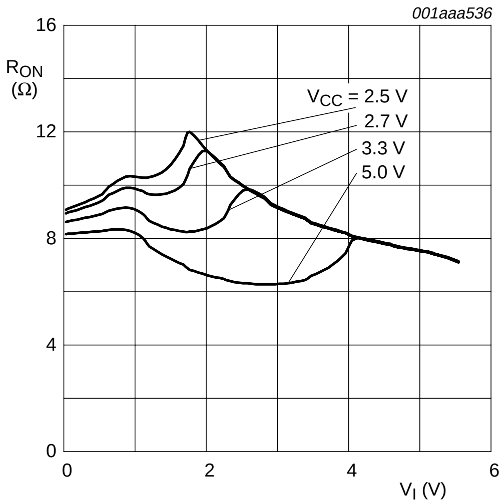
[2] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

10.3 ON resistance test circuit and graphs



V_I = GND to 5.5 V; $R_{ON} = V_{SW} / I_{SW}$.

Fig 8. Test circuit for measuring ON resistance



V_I = GND to 5.5 V; T_{amb} = 25 °C.

Fig 9. Typical ON resistance as a function of input voltage

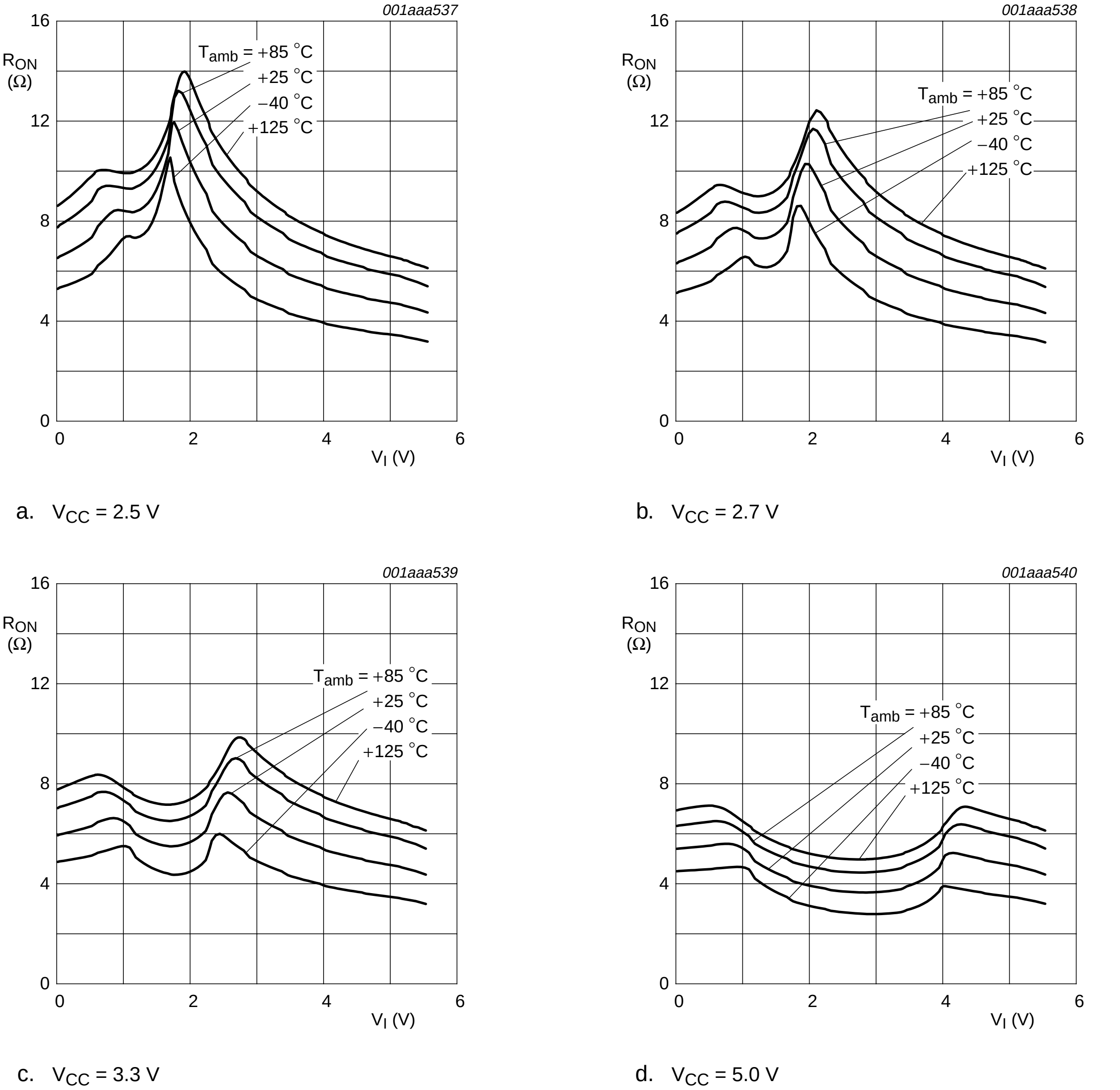


Fig 10. ON resistance as a function of input voltage at various supply voltages

11. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 13.

Symbol	Parameter	Conditions		−40 °C to +85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nY to nZ or nZ to nY; see Figure 11	[2][3]						
		V_{CC} = 2.3 V to 2.7 V		-	0.4	1.2	-	2.0	ns
		V_{CC} = 2.7 V		-	0.4	1.0	-	1.5	ns
		V_{CC} = 3.0 V to 3.6 V		-	0.3	0.8	-	1.5	ns
		V_{CC} = 4.5 V to 5.5 V		-	0.2	0.6	-	1.0	ns
t_{en}	enable time	nE to nY or nZ; see Figure 12	[4]						
		V_{CC} = 2.3 V to 2.7 V		1.0	4.7	12	1.0	15	ns
		V_{CC} = 2.7 V		1.0	4.4	8.5	1.0	11	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	3.8	7.5	1.0	9.5	ns
		V_{CC} = 4.5 V to 5.5 V		1.0	2.7	5.0	1.0	6.5	ns
t_{dis}	disable time	nE to nY or nZ; see Figure 12	[5]						
		V_{CC} = 2.3 V to 2.7 V		1.0	6.0	16	1.0	20	ns
		V_{CC} = 2.7 V		1.0	7.9	15	1.0	19	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	6.5	13.5	1.0	17	ns
		V_{CC} = 4.5 V to 5.5 V		1.0	4.4	9.0	1.0	11.5	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 10 MHz; V_I = GND to 5.5 V	[6]						
		V_{CC} = 2.5 V		-	9.7	-	-	-	pF
		V_{CC} = 3.3 V		-	10.3	-	-	-	pF
		V_{CC} = 5.0 V		-	11.3	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified capacitance when driven by an ideal voltage source (zero output impedance).

[4] t_{en} is the same as t_{PZH} and t_{PZL}.

[5] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[6] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma\{(C_L + C_{S(ON)}) \times V_{CC}^2 \times f_o\}$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

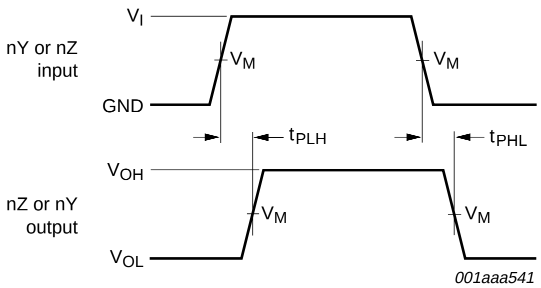
$C_{S(ON)}$ = maximum ON-state switch capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma\{(C_L + C_{S(ON)}) \times V_{CC}^2 \times f_o\}$ = sum of the outputs.

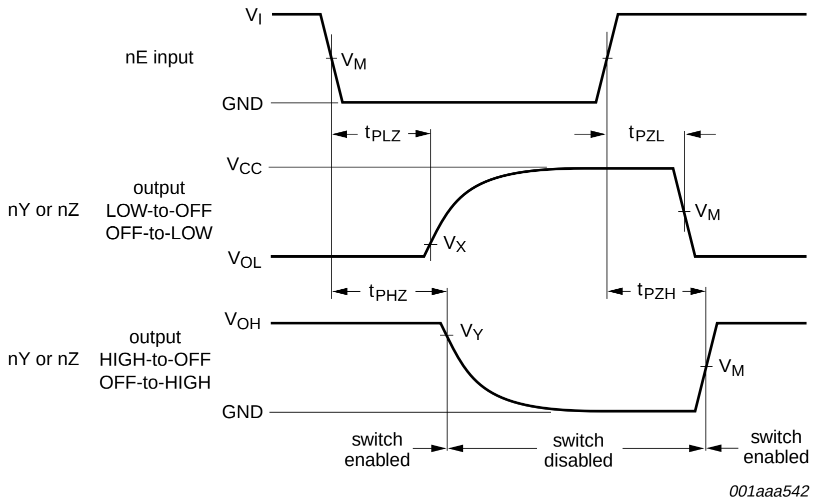
11.1 Waveforms and test circuit



Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 11. Input (nY or nZ) to output (nZ or nY) propagation delays



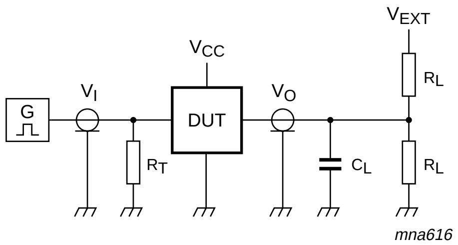
Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 12. Enable and disable times

Table 10. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} – 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} – 0.3 V
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} – 0.3 V



Test data is given in Table 11.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

V_{EXT} = External voltage for measuring switching times.

Fig 13. Load circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	$2V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6.0 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6.0 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2V_{CC}$

11.2 Additional dynamic characteristics

Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

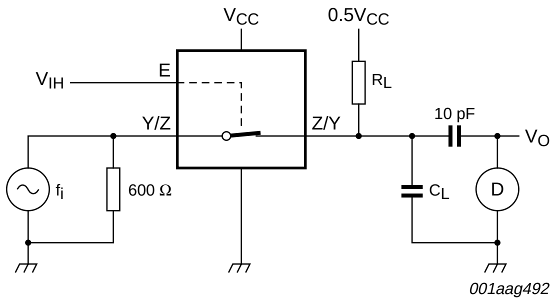
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	f_i = 1 kHz; R_L = 10 kΩ; C_L = 50 pF; see Figure 14				
		V_{CC} = 2.3 V	-	0.42	-	%
		V_{CC} = 3.0 V	-	0.36	-	%
		V_{CC} = 4.5 V	-	0.47	-	%
		f_i = 10 kHz; R_L = 10 kΩ; C_L = 50 pF; see Figure 14				
		V_{CC} = 2.3 V	-	0.11	-	%
		V_{CC} = 3.0 V	-	0.07	-	%
		V_{CC} = 4.5 V	-	0.01	-	%

Table 12. Additional dynamic characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{(-3dB)}$	–3 dB frequency response	R_L = 600 Ω; C_L = 50 pF; see Figure 15				
		V_{CC} = 2.3 V	-	160	-	MHz
		V_{CC} = 3.0 V	-	200	-	MHz
		V_{CC} = 4.5 V	-	210	-	MHz
		R_L = 50 Ω; C_L = 5 pF; see Figure 15				
		V_{CC} = 2.3 V	-	180	-	MHz
		V_{CC} = 3.0 V	-	180	-	MHz
		V_{CC} = 4.5 V	-	180	-	MHz
α_{iso}	isolation (OFF-state)	R_L = 600 Ω; C_L = 50 pF; f_i = 1 MHz; see Figure 16				
		V_{CC} = 2.3 V	-	–65	-	dB
		V_{CC} = 3.0 V	-	–65	-	dB
		V_{CC} = 4.5 V	-	–62	-	dB
		R_L = 50 Ω; C_L = 5 pF; f_i = 1 MHz; see Figure 16				
		V_{CC} = 2.3 V	-	–37	-	dB
		V_{CC} = 3.0 V	-	–36	-	dB
		V_{CC} = 4.5 V	-	–36	-	dB
V_{ct}	crosstalk voltage	between digital inputs and switch; R_L = 600 Ω; C_L = 50 pF; f_i = 1 MHz; t_r = t_f = 2 ns; see Figure 17				
		V_{CC} = 2.3 V	-	91	-	mV
		V_{CC} = 3.0 V	-	119	-	mV
		V_{CC} = 4.5 V	-	205	-	mV
Xtalk	crosstalk	between switches; R_L = 600 Ω; C_L = 50 pF; f_i = 1 MHz; see Figure 18				
		V_{CC} = 2.3 V	-	–56	-	dB
		V_{CC} = 3.0 V	-	–55	-	dB
		V_{CC} = 4.5 V	-	–55	-	dB
		between switches; R_L = 50 Ω; C_L = 5 pF; f_i = 1 MHz; see Figure 18				
		V_{CC} = 2.3 V	-	–29	-	dB
		V_{CC} = 3.0 V	-	–28	-	dB
		V_{CC} = 4.5 V	-	–28	-	dB
Q_{inj}	charge injection	C_L = 0.1 nF; V_{gen} = 0 V; R_{gen} = 0 Ω; f_i = 1 MHz; R_L = 1 MΩ; see Figure 19				
		V_{CC} = 2.5 V	-	< 0.003	-	pC
		V_{CC} = 3.3 V	-	0.003	-	pC
		V_{CC} = 4.5 V	-	0.0035	-	pC
		V_{CC} = 5.5 V	-	0.0035	-	pC

11.3 Test circuits



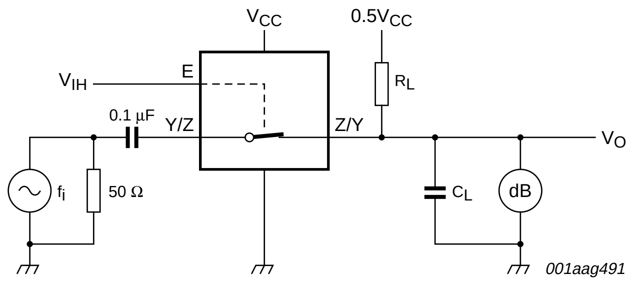
Test conditions:

V_{CC} = 2.3 V: V_i = 2 V (p-p).

V_{CC} = 3 V: V_i = 2.5 V (p-p).

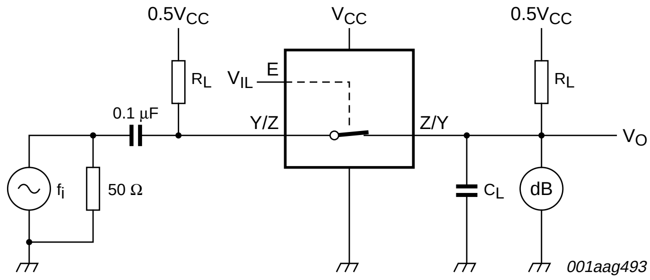
V_{CC} = 4.5 V: V_i = 4 V (p-p).

Fig 14. Test circuit for measuring total harmonic distortion



Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads –3 dB.

Fig 15. Test circuit for measuring the frequency response when switch is in ON-state



Adjust f_i voltage to obtain 0 dBm level at input.

Fig 16. Test circuit for measuring isolation (OFF-state)

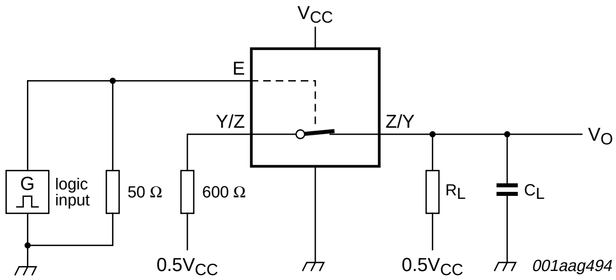
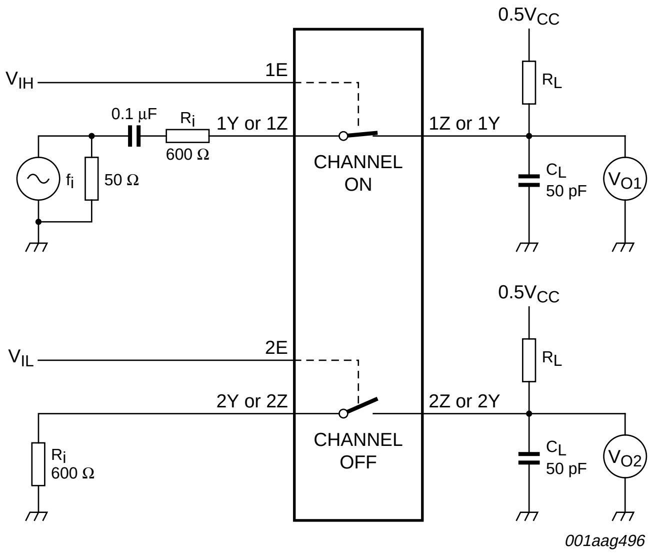
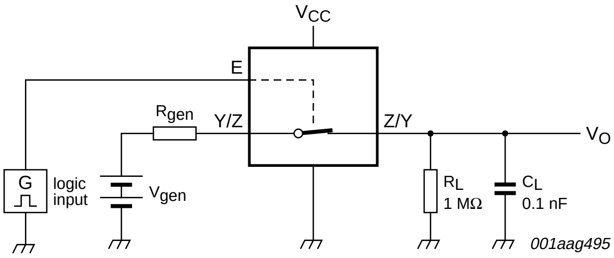


Fig 17. Test circuit for measuring crosstalk voltage (between digital inputs and switch)

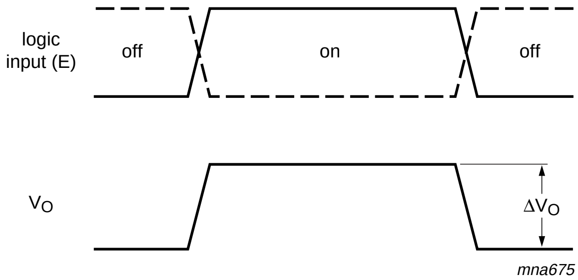


$20 \log_{10} (V_{O2} / V_{O1})$ or $20 \log_{10} (V_{O1} / V_{O2})$.

Fig 18. Test circuit for measuring crosstalk between switches



a. Test circuit



b. Input and output pulse definitions

$Q_{inj} = \Delta V_O \times C_L$.

ΔV_O = output voltage variation.

R_{gen} = generator resistance.

V_{gen} = generator voltage.

Fig 19. Test circuit for measuring charge injection

12. Application information

Use the 74LVCV2G66 to reduce component count and footprint in low-power portable applications.

Typical ‘66’ devices do not have low-power enable inputs causing a high ΔI_{CC}. To reduce power consumption in portable (battery) applications, a current limiting resistor is used. (see Figure 20a). The low-power enable inputs of the 74LVCV2G66 have much lower ΔI_{CC}, eliminating the necessity of the current limiting resistor (see Figure 20b).

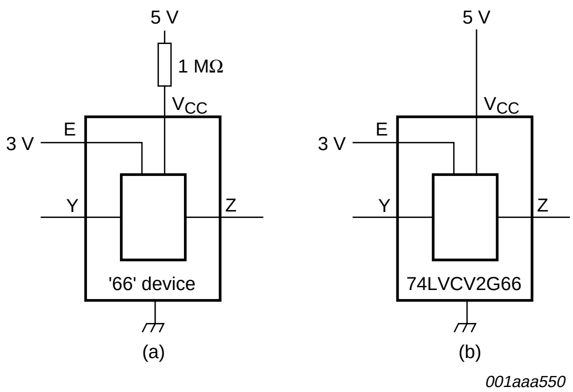
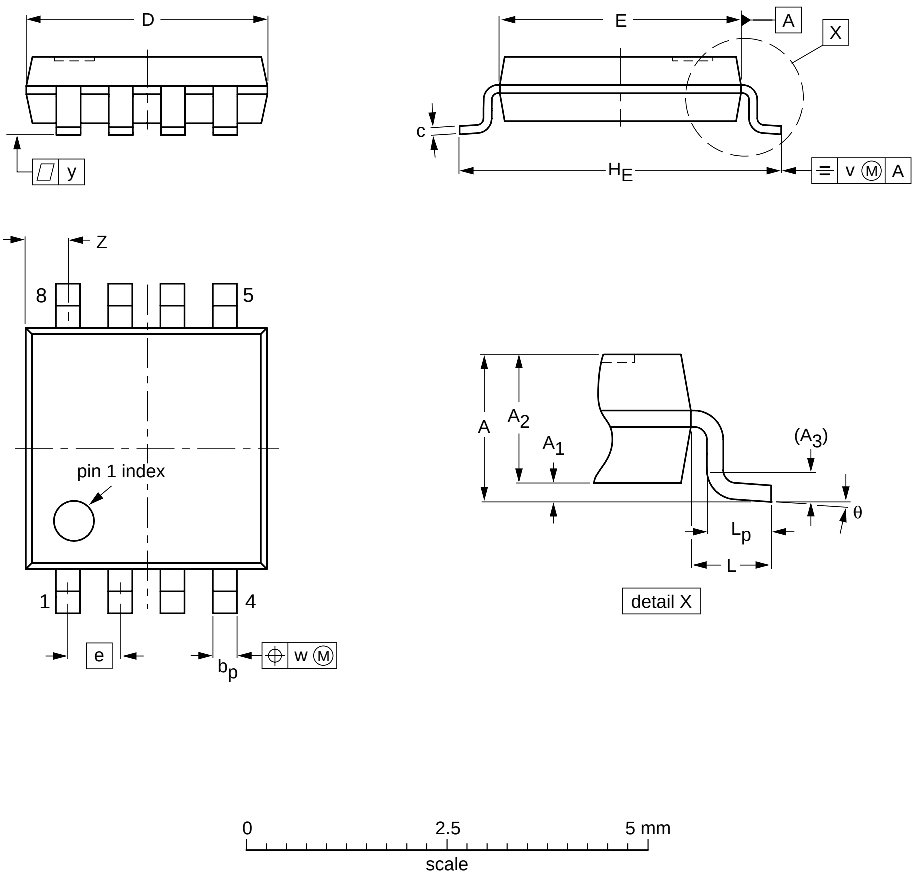


Fig 20. Application example

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm **SOT505-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	v	w	y	Z(1)	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

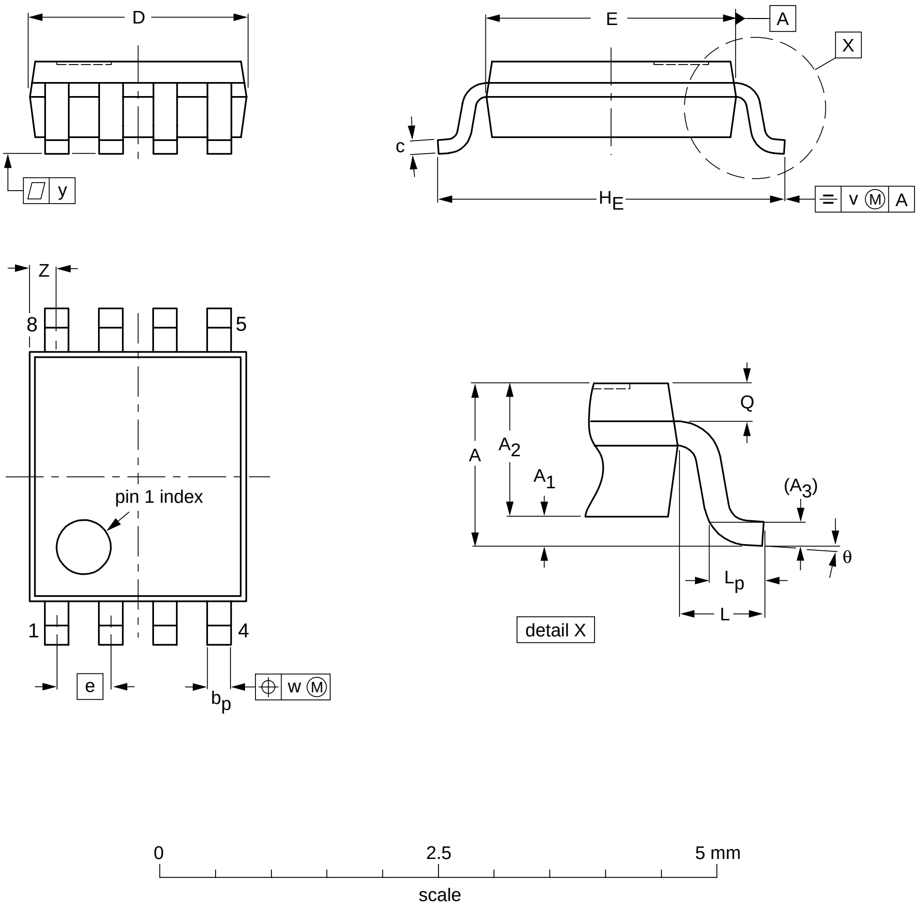
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig 21. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

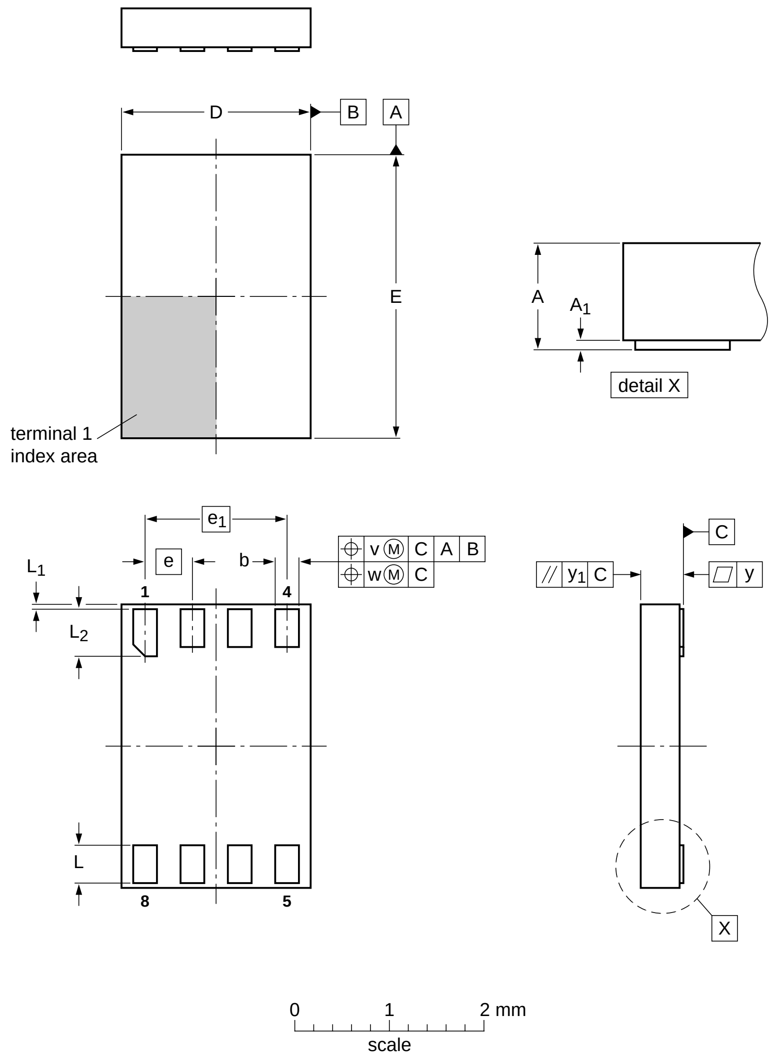
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Fig 22. Package outline SOT765-1 (VSSOP8)

XSON8U: plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body 3 x 2 x 0.5 mm **SOT996-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	b	D	E	e	e_1	L	L_1	L_2	v	w	y	y_1
mm	0.5	0.05 0.00	0.35 0.15	2.1 1.9	3.1 2.9	0.5	1.5	0.5 0.3	0.15 0.05	0.6 0.4	0.1	0.05	0.05	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT996-2	- - -		- - -			~~07-12-18~~ 07-12-21

Fig 23. Package outline SOT996-2 (XSON8U)

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test

15. Revision history

Table 14: Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVCV2G66_2	20080703	Product data sheet	-	74LVCV2G66_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Added type number 74LVCV2G66GD (XSON8U package).			
74LVCV2G66_1	20040402	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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Document identifier: 74LVCV2G66_2